CDAC ARCHITECTURE PLUS RESISTOR DIVIDER GIVES ADC574 PINOUT WITH SAMPLING, LOW POWER, NEW INPUT RANGES

George Hill (602) 746-7283

Modern successive-approximation analog-to-digital converter ICs are replacing older current-mode D/A structures with capacitor arrays, called CDACs (for Capacitor D/A). This change makes it easier to combine the analog components of the converter with the digital elements in standard CMOS structures. Additionally, the capacitor input structure adds inherent sampling to the A/D, at a time when more and more A/D applications are involved in signal processing.

This application note compares basic current-mode successive approximation A/Ds with CDAC-based architectures, and shows how adding a resistor divider network to the CDAC input permits the Burr-Brown ADS574 and ADS774 to fit existing ADC574 sockets. It then goes on to describe some new analog input voltage ranges available on these parts due to the resistor network and CDAC approach.

The ADS574 and ADS774 plug into ADC574/674/774 sockets and handle all of their standard input ranges (0V to 10V, ±5V, ±10V, and 0V to 20V), as discussed in their full data sheets. They can operate from standard ±15V and +5V supplies, or from a single +5V supply. The input divider structure makes it possible to take advantage of this +5V supply operation to build complete data acquisition systems that run from a single +5V supply, with several different input ranges pin-selectable.

TRADITIONAL ADC574 INPUT STRUCTURE

Let's start by taking a look at the input ranges on the traditional ADC574, the most widely used 12-bit A/D in the world. Figure 1 shows the standard input divider network and comparator/current D/A structure used to implement the front end of this successive approximation A/D.
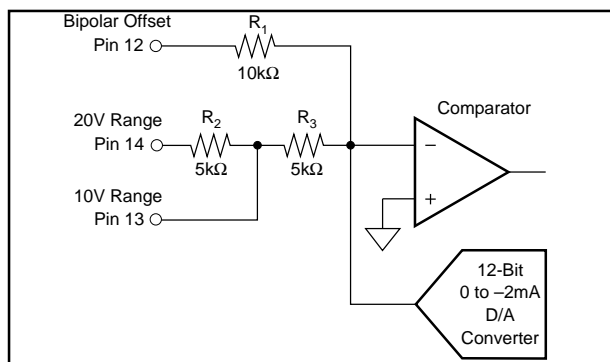
These three pins allow the selection of four different analog input ranges: 0V to +10V, 0V to +20V, ±5V, and ±10V. The simplicity of this circuit takes advantage of the virtual ground at the negative input to the comparator at the end of the successive approximation process, when the negative input to the comparator is very close to 0V.

The internal current D/A in the ADC574 has a unipolar output of 0mA to –2mA, so that it can balance out the 0mA to 2mA generated by full scale analog inputs (20V across 10kΩ or 10V across 5kΩ.) By grounding pin 12, a unipolar 0V to 20V input range is achieved by driving pin 14 and leaving pin 13 unconnected. Reversing pins 13 and 14 sets up the ADC574 for a 0V to 10V input range.

Connecting pin 12 to the 10V, reference provided on an ADC574 injects an offset that allows pins 13 or 14 to handle bipolar input ranges of ±5V or ±10V, respectively. The current injected by the reference at pin 12 adds to the input current generated by the analog input signal to insure that the unipolar current flow from the internal current D/A need only be unipolar.

During conversion, the analog signal conditioning in a system must hold the input stable (using a sample/hold amplifier or processing slow signals such as thermocouples.) The successive approximation logic tests the current D/A in various settings until the current sinked into the D/A balances the current generated by the analog input signal (plus the current from the Bipolar Offset resistor in bipolar ranges) to within ±1/2 LSB.

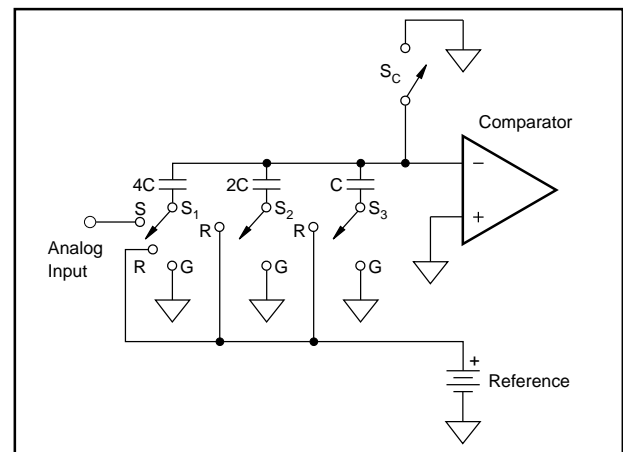FIGURE 1. Traditional ADC574 Input Structure.

FIGURE 2. Simplified 3-bit Switched Capacitor Array A/D.

BASIC SWITCHED CAPACITOR ARRAY A/D

By comparison, Figure 2 shows a typical input structure for a switched capacitor array used to implement a successive approximation A/D in CMOS. For simplification, a 3-bit converter is shown in Figure 2. When not converting, switch S_1 (to the MSB capacitor) is in the "S" position so that the charge on the MSB capacitor is proportional to the voltage level of the analog input signal. Switches S_2 and S_3 are in the "G" position, and switch S_C is closed, setting the comparator input offset to zero. A convert command opens switches S_1 and S_C, to trap a charge on the MSB capacitor and to float the comparator input. During the conversion, switches S_1, S_2 and S_3 are successively tested in various "R" and "G" positions to find the combination that sets the comparator input closest to 0V, thus balancing the charge.

For our discussion, the critical condition occurs during the sampling phase, when the analog charge proportional to the analog input voltage is captured. The analog input is driving a capacitor, effectively an extremely high impedance. This is just the opposite of driving a virtual ground, which is where the comparator input in traditional ADC574s is at the end of the conversion process.

ADS574 INPUT STRUCTURE

The desire to use a CDAC architecture to develop an A/D that can drop into ADC574 sockets was a major design challenge. Figure 3 shows the resistor divider network that meshes the analog input ranges of the standard ADC574 with a CDAC to produce the ADS574, a single-supply, sampling A/D that plugs into most existing ADC574 sockets with no changes required to either hardware or software.
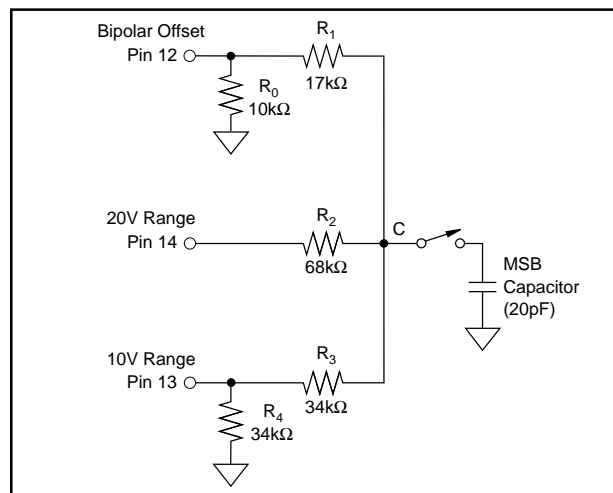

FIGURE 3. ADS574 Input Structure.

The full-scale voltage range for the MSB input capacitor on the ADS574 was designed to be 0V to +3.33V. This meant that the input resistor divider network had to provide the standard ADC574 input ranges using the same three pins, and also scale the voltage at the MSB capacitor to the 0V to 3.33V range. The on-chip laser-trimmed nichrome input resistors solve the problem of handling 20V analog signals, unipolar or bipolar, in a converter using a single +5V supply and ground as its rails.

The 5V supply means that the ADS574 does not provide a 10V reference, but instead provides a 2.5V reference output. The Bipolar Offset input, pin 12, had to be designed for this 2.5V reference, but also had to be designed to ensure that standard ADC574 offset adjust trim circuits produce similar trim results and range. This offset trim compatibility is the primary role of the 10kΩ resistor R_0 at pin 12.

For unipolar input ranges without offset trim circuits, standard ADC574s have pin 12 connected to analog common, which the ADS574 emulates. In the standard ADC574, R_1 in Figure 1 is essentially out of the equation for the input divider network as the comparator input approaches 0V during the successive approximation process. In the ADS574, R_1 in Figure 3 always plays a significant role.

For the 0V to 20V unipolar input range on the ADS574, as on the standard ADC574, pin 12 is grounded, pin 13 is left open, and the analog input is applied to pin 14. Since the input to the MSB capacitor on the ADS574 is very much higher than the input resistors, only R_1, R_2, R_3 and R_4 in Figure 3 determine the voltage at C for a given input voltage at pin 14. (The 10kΩ R_0 is grounded at both ends, and can thus be ignored.)

An analog input at pin 14 is divided by 6 at point C as follows:

Equation 1

$$V_C = \frac{(R3 + R4) \parallel R1}{R2 + [(R3 + R4) \parallel R1]} \bullet V_{IN}$$

$$V_C = 1/6 \ V_{IN}$$

This matches a 0V to 20V input range at pin 14 to the 0V to 3.33V range required by the ADS574 internally.

In the unipolar 0V to 10V range, pin 12 is again connected to ground, and pin 14 is unconnected. This case is simpler to analyze, since neither R_2 nor R_4 have any effect on the voltage at C. In this case, the analog input at pin 13 is divided by 3 at point C.

The bipolar input ranges are also more complicated on the ADS574 than on standard ADC574s. The ADS574 uses the same external trimpots or fixed resistors already present in ADC574 sockets for bipolar offset, but works with the internal 2.5V reference.

For the ±10V input range without external offset trim, standard ADC574s have pin 12 connected to the +10V reference (internal or external) through a 50Ω resistor. Pin 13 is again left unconnected, and the analog signal to be

digitized is input at pin 14. The ADS574 uses the same input connections. As above, the input to the MSB capacitor on the ADS574 has very much higher impedance than the resistor divider network. Thus, in Figure 3, R_1, R_2, R_3, R_4, plus the reference voltage at pin 12, determine the voltage at C for a given input voltage at pin 14 (assuming the reference source impedance is much lower than R_1 and R_0).

An analog input voltage at pin 14 is divided and offset at point C as follows:

Equation 2

$$\frac{V_{IN} - V_C}{R_2} = \frac{V_C}{R_3 + R_4} + \frac{V_C - 2.5}{R_1}$$

Solving for V_C, the voltage at point C, in terms of V_{IN}, the voltage at pin 14, gives:

Equation 3

$$V_C = 1/6\ V_{IN} + 1.67$$

For a –10V input at pin 14, point C is again 0V, and a +10V input at pin 14 generates 3.33V at point C. The reference input at pin 12 sources current when the analog input at pin 14 is less than 1.67V, and sinks current when it is greater than 1.67V.

For the bipolar ±5V input range without offset trim, pin 12 is again connected to the reference (internal or external) through a 50Ω resistor on both the traditional ADC574 and the ADS574. In this case, pin 14 is left unconnected, so that R_2 has no effect on the voltage at point C. R_4 also has no effect. The voltage at point C is simply:

Equation 4

$$V_C = 1/3\ V_{IN} + 1.67$$

A –5V input at pin 13 generates 0V at point C, a 0V input generates 1.67V (half-scale), and +5V generates 3.33V (full-scale.)

NEW INPUT RANGES
ALLOWED BY THE ADS574[1]

Because of the widespread use of the traditional ADC574, there exists large amounts of software and digital interface hardware built around this pinout. The ADS574 input structure lets this existing software and hardware be easily applied in systems requiring different analog input ranges. Since the ADS574 can operate from a single +5V supply, perhaps the most interesting optional input range is 0V to +5V. Figure 4 shows how to achieve this range. The analog input signal is driven, through a fixed 50Ω resistor, into pin 12 (the Bipolar Offset pin), with pin 14 (the 20V Range Input) grounded, and pin 13 (the 10V Range Input) unconnected. The input signal at pin 12 is divided by the network

of $R_1 + (R_2 \| (R_3 + R_4))$. Point C is at the internal full-scale 3.33V when 5V is input at pin 12, and is 0V when 0V is input at pin 12. Using the ADS574 connected as shown in Figure 4 would allow building a complete sampling A/D system running off a single +5V supply, limited only by how close other analog input circuitry can get to ground or the supply.

Tests in the lab using the connections shown in Figure 4, and the other circuits shown below where pin 12 is used as an input, confirm the operation of these circuits, although with slight degradation in linearity. The ADS574 in these modes maintains 12-bit differential linearity, with No Missing Codes at the 12-bit level, but integral linearity is at the 10- to 11-bit level. The degradation from ideal performance has been traced to a circuit design that was required to maximize compatibility in existing ADC574 sockets. This circuit can easily be modified to enhance performance in these input ranges, if needed.
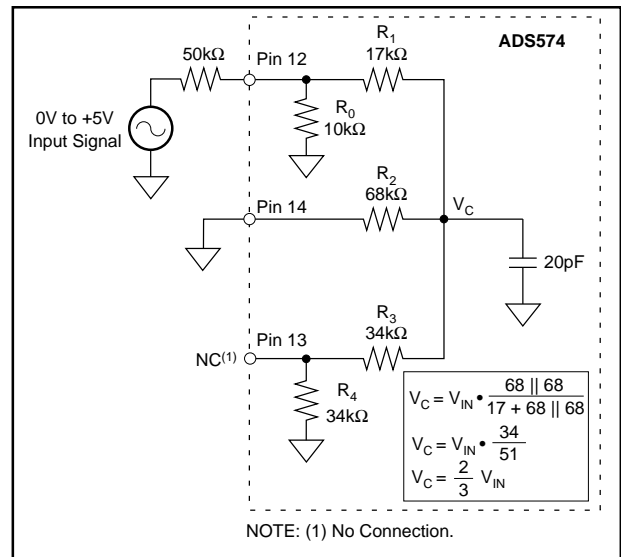

FIGURE 4. Connections for 0V to +5V Input Range.

Some operational amplifiers capable of running off a single +5V supply can swing closer to 0V than to the +5V supply. Figure 5 shows how to configure the ADS574 for a 0V to +3.33V input range to better utilize the dynamic range of such amplifiers. By connecting pins 12, 13 and 14 all to the input signal, there is no divider network between the input and point C, so that the input voltage will also be the voltage at point C. (Once again, this is based on the very high input impedance of the 20pF MSB capacitor internal to the ADS574.)

For bipolar signals in systems with supply voltages limited to ±5V, the connections in Figure 6 can be used to handle a ±2.5V input signal. The analog input signal is applied to pin 12, with pin 14 left unconnected. Connecting pin 13 to the

+5V supply offsets the voltage at point C generated by an input signal at pin 12 so that the voltage range at point C is again the 0V to 3.33V required internally. Obviously, any ripple or variation on the +5V supply line will feed straight through the divider network, and be converted by the ADS574. For this approach to work, the +5V supply needs to be stable enough to maintain the system accuracy required. If there is a stable +5V reference available in the system, it could also be used to generate the bipolar offset, and perhaps even power the ADS574, which consumes only 100mW maximum.
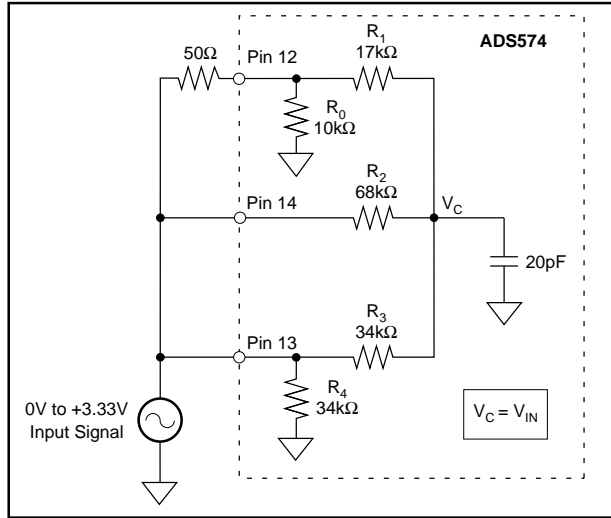

FIGURE 5. Connections for 0V to +3.33V Input Range.

For applications needing maximum integral linearity with a 0V to 5V input range, Figure 7 shows the optimal connections. This avoids the slight degradation of integral linearity mentioned above when pin 12 is used as an input pin, but sacrifices about 35% of the A/Ds output codes (the codes for inputs from 5V to 7.778V.) Using a K-grade ADS574 in this configuration will yield better than 11-bit resolution (2633 codes) and integral linearity from 0V to 5V, since it has ±1/2LSB integral linearly over the 0V to +7.778V input range.

The ADS574 input structure was optimized for compatibility with ADC574 sockets, and was not designed or characterized for these additional input ranges. However, the simplicity of the input resistor divider network makes it straight-forward to see how they work. For all of these additional input ranges, the standard trim circuitry for gain adjust (not discussed above but described in the ADS574 data sheet) can still be used to adjust full-scale range. To trim offset error, it is probably advisable to trim elsewhere in the system. In most systems, there will be an op amp in front of the ADS574, and it should be simple to trim out the system offset by adjusting the offset of this amplifier.

CMOS VS BiCMOS

It should be noted that the CDAC architecture used in the ADS574 and ADS774 is not the only possible way to implement a monolithic sampling A/D in the standard ADC574 pinout. One alternative is the BiCMOS-based Analog Devices AD1674. Analog Devices chose to stick with the current-mode DAC for the A/D section of their sampling ADC574 replacement, and to add a true sample/hold amplifier to the front end of the converter. To accomplish this in a monolithic chip, they applied a BiCMOS process. Burr-Brown chose to use standard CMOS processing and a CDAC. The results of these two approaches are compared with each other and with the standard ADC574 and ADC774 in Table I.

Basically, the process chosen by Burr-Brown takes advantage of the power savings offered by CMOS, and turns out to allow new input ranges and the possibility of new data acquisition applications using a single +5V supply for the entire system. The only ADC574 compatibility concern is in systems where either an external 10V reference drives the A/D reference input, or where the internal 10V reference is used elsewhere. The Analog Devices AD1674 maintains the reference compatibility, but actually increases power consumption to achieve this (and to build a traditional sample/hold amplifier.)
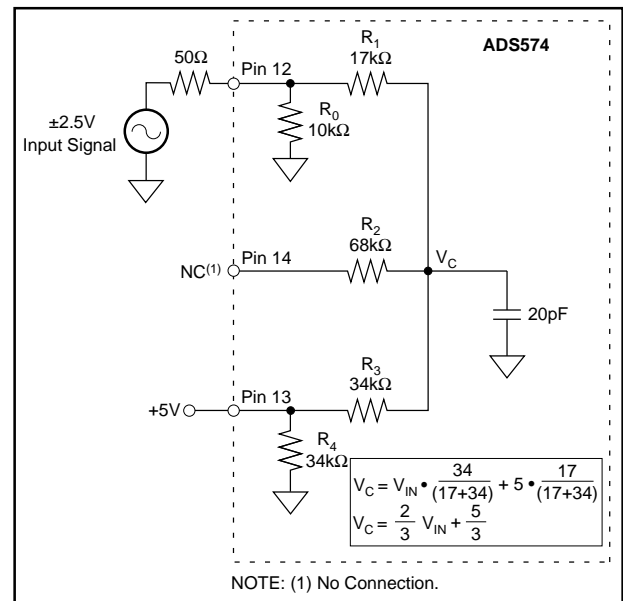

FIGURE 6. Connections for ±2.5V Input Range.

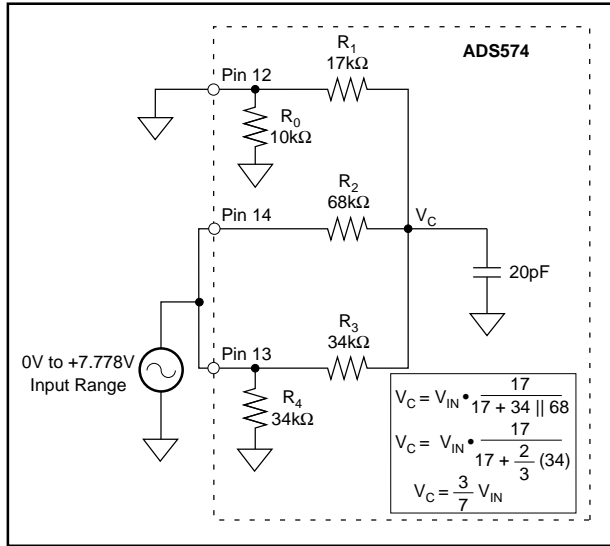FIGURE 7. Connections for 0V to +7.778V Input Range.

	ADC574	ADS574	ADC774	ADS774	AD1674
Standard Input Ranges	0V to 10V, ±5V, 0V to 20V, ±10V	0V to 10V, ±5V, 0V to 20V, ±10V	0V to 10V, ±5V, 0V to 20V, ±10V	0V to 10V, ±5V, 0V to 20V, ±10V	0V to 10V, ±5V, 0V to 20V, ±10V
New Input Ranges	None	0V to 7.778V, ±2.5V[1], 0V to 5V[1], 0V to 3.33V[1]	None	0V to 7.778V, ±2.5V[1], 0V to 5V[1] 0V to 3.33V[1]	None
Typ Input Impedance: 10V Ranges 20V Ranges	5kΩ 10kΩ	21kΩ 84kΩ	5kΩ 10kΩ	12kΩ 50kΩ	5kΩ 10kΩ
Min Input Impedance: 10V Ranges 20V Ranges	4.7kΩ 9.4kΩ	15kΩ 60kΩ	4.7kΩ 9.4kΩ	8.5kΩ 35kΩ	3kΩ 6kΩ
Max LSBs Integral Non-Linearity Error (J,K)	±1, ±1/2	±1, ±1/2	±1, ±1/2	±1, ±1/2	±1, ±1/2
No-Missing Codes Resolution	11-bits (Js)	12-bits	11-bits (Js)	12-bits	12-bits
Min Signal-to-(Noise + Distortion) Ratio with 10kHz Input (J/K Grades)	N/A	68/70dB	N/A	68/70 dB	69/70 dB
Max Conversion Time Over Temperature	25µs		8.5µs		
Max Acquisition and Conversion Time Over Temperature		25µs		8.5µs	10µs
Reference Output/Input	+10V	+2.5V	+10V	+2.5V	+10V
Power Supplies Required	±12 to 15V, +5V	+5V	±12 to 15V, +5V	+5V	±12 to 15V, +5V
Max Power Dissipation	450mW	100mW	450mW	120mW	575mW
Packages Available	0.6" DIPs and PLCC	0.6" and 0.3" DIPs, SOIC, Die	0.6" DIPs and PLCC	0.6" and 0.3" DIPs, SOIC, Die	0.6" DIPs Contact Factory for Surface Mount
Able to Emulate ADC574 Timing	Yes	Yes	Yes	Yes	No
Able to Fully Control S/H Timing	N/A	Yes	N/A	Yes	Yes
Able to Operate From Single +5V Supply	No	Yes	No	Yes	No
NOTE: (1) With slightly degraded integral linearity, as described in the text.					

TABLE I. Comparing Burr-Brown ADC574, ADC774, ADS574 and ADS774 with Analog Devices AD1674.